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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Divakaruni et al.

Serial No. 09/718,850 Group Art Unit: 2811

Filed: November 11, 2000 Examiner: Gebremariam, Samuel A.

For: LOGIC STRUCTURE PROCESS AND APPLICATION FOR VERTICLE BIPOLAR TRANSISTOR

Assistant Commissioner of Patents
Washington, D.C. 20231

AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

In response to the Office Action mailed January 22, 2003, please amend the above-identified patent application as follows:

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to the Assistant Commissioner for Patents, Washington, DC 20231 on April 22, 2003.

Frederick W. Gibb, III